REMARKS/ARGUMENTS

In the Office Action mailed March 13, 2008, claims 1-11 were rejected. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended, added, or canceled.

Withdrawal of Finality

As a preliminary matter, Applicants respectfully note that the finality of the present Office Action should be withdrawn because this Office Action presents the first rejection of claim 6. In particular, Applicants previous response noted that the prior Office Action did not present a rejection for claim 6. Furthermore, although the present Office Action states that the finality is based on a new rejection necessitated by Applicants' amendments, this rejection of claim 6 is nevertheless the first rejection presented for claim 6.

The MPEP states that a second action on the merits shall be final, except where the Examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims, nor based on information submitted in an information disclosure statement. MPEP 706.07(a). In other words, the status of a second or later action may be made final, even if there is a new rejection that is different from an initial rejection, if the new rejection was prompted by an amendment by the applicant. Hence, the reference to "a new ground of rejection" implies that there must have been a previous rejection of the claim.

Here, the Examiner presents the finality of the present Office Action in reliance on an amendment to the claims as the basis for a new ground of rejection. However, Applicants respectfully submit that the present rejection of claim 6 should not be considered a new ground of rejection because no rejections for claim 6 have been presented previously in this case. Thus, regardless of whether or not the current rejection might take into account the amendments to independent claim 1, the current rejection of claim 6 is the first and only rejection that has been presented for claim 6. Since this is the first and only rejection of claim 6, Applicants have only been presented with a single opportunity to discuss the patentability of claim 6 over an asserted rejection of the claim.

Therefore, Applicants respectfully request that the finality of the present Office Action be withdrawn because this is the first and only ground of rejection presented for claim 6.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1, 2, 4, 5, and 7-11 were rejected under 35 U.S.C. 102(b) as being anticipated by Emma et al. (U.S. Pat. No. 5,584,002, hereinafter Emma). Additionally, claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Asher (U.S. Pat. No. 6,671,822, hereinafter Asher). Additionally, claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Kramer (U.S. Pat. No. 4,868,869, hereinafter Kramer). However, Applicants respectfully submit that these claims are patentable over Emma, Asher, and Kramer for the reasons provided below.

Independent Claim 1

Claim 1 recites "remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first bank of memory modules to a second bank of memory modules" (emphasis added).

While the details of the specification are not read into the limitations of the claim, it may be useful to refer to the specification of the present application for a contextual understanding of the limitations recited in the claim. The specification of the present application describes a cache such as a level 2 (L2) cache for use with one or more processors. Page 5, lines 3-11; Fig. 1. The L2 cache is partitioned into several (e.g., 8) banks, which are referred to as a shared L2 cache, L2_bank. Id. Each bank can serve a read or write request independently from the other banks. Page 5, lines 12-20. This independence means that there can be concurrent transfers for each of the 8 banks. Id. Each bank is partitioned in six ways. Id. Only one way can be active in a bank at a given time. Id. Thus, the specification provides some description that illustrates how the banks are partitions of, for example, the L2 cache. Moreover, the banks have a specific relationship with the L2 cache and the ways partitions implemented in each bank. Additionally, a specific signal (i.e., the bank_select signal) is used for selecting one of the several banks. Page 6, lines 24-25.

Also, it should be understood that the banks and memory modules described in the present application refer to physical devices. In particular, the banks and memory modules of the L2 cache are described as being connected to a coherent interconnection network (CIN) for connection to other hardware such as the processing units (TM) and the controller (DDR_ctrl). Additionally, the specification of the present application explains that the L2 cache, which includes the partitioned banks and memory modules, may be implemented as embedded dynamic random access memory (DRAM) modules. DRAM modules, which are known in the art, are physical hardware components that implement the physical banks of memory modules. Thus, the references to banks and memory modules in the present application, including the references in claim 1, should be understood as referring to physical components.

In contrast to the indicated limitation of claim 1, Emma does not disclose remapping memory modules from one bank to another bank of memory modules. Emma merely addresses the historic cache synonym problem in which address references within a cache synonym class ambiguously reference addresses which have the same non-translatable address field but different translatable address bits. Emma, col. 2, line 63, through col. 3, line 9. More specifically, Emma describes a cache system to remap data in response to a hardware failure that disables a congruence class. Emma, col. 3, lines 54-59. A congruence class simply identifies a limited group of locations in the cache at which data from a given memory address may be stored. Emma, col. 1, lines 39-42. In particular, each row within the cache forms a congruence class. Emma, col. 1, lines 61-63.

Emma further explains that the loss of a single storage element in a set associative cache only disables one set of the congruence class. Emma, col. 2, lines 46-48. Additionally, Emma explains that it is possible to increase the number of congruence classes without changing set associativity. Emma, col. 2, lines 53-56. This description illustrates that the congruence classes are merely logical designations, rather than physical components within the cache.

In support of the rejection of claim 1, the Office Action attempts to draw a correlation between the disclosed congruence classes of Emma and the memory modules and banks of the present application. In particular, the Office Action states that "each

bank corresponds to a congruence class in Emma." Office Action, 3/13/08, p. 3. Thus, according to the Office Action, remapping data from a first congruence class to a second congruence class is purportedly the equivalent of going from a first bank to a second bank.

However, this characterization presented in the Office Action does not appear to recognize the inherent differences between the logical congruence classes of Emma and the physical memory modules and banks of the present application. Rather, the congruence classes of Emma are not first and second banks, as recited in the claim, because the congruence classes are merely logical designations and are not physical banks of memory modules within the cache.

Moreover, there is no explanation in Emma to support the assertion presented in the Office Action that there might be a specific relationship between logical congruence classes and physical banks of memory modules. In fact, there appears to be no support in Emma for this assertion. Additionally, the Office Action fails to provide any evidence or reasoning to support the assertion that physical banks of memory modules purportedly correspond to the logical congruence classes in Emma. Rather, the Office Action merely asserts an unsupported conclusion, without providing evidence of the asserted correspondence or reasoning to explain in detail how the physical banks of memory modules might correspond to the logical congruence classes described in Emma.

Therefore, since the logical congruence classes in Emma are not physical banks of memory modules, and there is no evidence or reasoning to support the assertion that there might be some correspondence between the logical congruence classes and the physical banks of memory modules, Emma does not disclose all of the limitations of the claim. Accordingly, Applicants respectfully submit claim 1 is patentable over Emma because Emma does not disclose all of the limitations of the claim.

Independent Claim 8

Applicants respectfully assert independent claim 8 is patentable over Emma at least for similar reasons to those stated above in regard to the rejections of independent claim 1. In particular, claim 8 recites "performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the

memory modules from a first bank of memory modules to a second bank of memory modules" (emphasis added).

Here, although the language of claim 8 differs from the language of claim 1, and the scope of claim 8 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejections of claim 1 also apply to the rejections of claim 8. Accordingly, Applicants respectfully assert claim 8 is patentable over Emma because Emma does not disclose remapping memory modules between banks of memory modules, as recited in the claim.

Dependent Claims

Claims 2-7 and 9-11 depend from and incorporate all of the limitations of independent claim 1. Applicants respectfully assert claims 2-7 and 9-11 are allowable based on an allowable base claim. Additionally, each of claims 2-7 and 9-11 may be allowable for further reasons.

In regard to claim 7, Applicants respectfully submit that claim 7 is patentable over Emma because Emma does not disclose all of the limitations of the claim. Claim 7 recites "a look up table for marking faulty memory modules" (emphasis added). In contrast, the cited portion of Emma (col. 9, lines 9-11) merely discloses detecting a hardware failure within a congruence class. More specifically, it should be understood that the hardware failure within the congruence class refers to a hardware failure of a physical component within the cache at a location corresponding to a congruence class. Nevertheless, the SC bit described in Emma is used to indicate a failed congruence class. There is no description in Emma of specifically marking a faulty memory module. Furthermore, there is no description in Emma that explains how to identify a faulty memory module using the SC bit because the SC bit merely provides an indication of a failed congruence class, generally, rather than a specific indication of a particular faulty memory module. Therefore, Emma does not disclose a look up table for marking faulty memory modules because Emma merely indicates a failed congruence class, generally. Accordingly, Applicants respectfully assert that claim 7 is patentable over Emma because Emma does not disclose all of the limitations of the claim.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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